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Inventor: Frederick P. Herrmann

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LIQUID CRYSTAL DISPLAY WITH INTEGRATED DIGITAL-ANALOG-CONVERTERS

RELATED APPLICATION

This application claims the benefit of U.S. Provisional Application No. 60/446,651, filed on February 11, 2003, the entire teachings of which are incorporated herein by reference.

BACKGROUND

Liquid crystal display (LCD) devices usually consist of two-dimensional arrays of thin-film circuit elements (pixels). Each pixel cooperates with liquid-crystal material to either transmit or prevent light travel through a column of liquid crystal material. The physical size of the pixel array is determined by the application.

A two-dimensional (2D) array, for example, can include two sets of conductive lines extending in perpendicular directions. Each line extending in one direction can provide signals to a column of the array; each line extending in another direction can provide signals to a row of the array.

Conventionally, each row-column position in a 2D array includes a pixel that responds to signals on the lines for the pixel's row and column combination. Through one set of parallel lines, illustratively called "data lines," each pixel receives signals that determine its state. Through the other set of parallel lines, illustratively called "scan lines," each pixel along a scan line receives a signal that enables the pixel to receive signals from its data line.

In conventional arrays, each scan line provides a periodic scan signal that enables a component in each pixel connected to the scan line to receive a signal from its

data line during a brief time interval of each cycle. Therefore, tight synchronization of the scan signals with signals on the data lines is critical to successful array operation. Tight synchronization in turn requires that the driving signals to the data lines be provided with precise timing.

The circuitry driving the data lines is termed the "data scanner." The circuitry driving the scan lines is termed the "select scanner."

The arrays are built on substrates, usually of glass or quartz. The pixel arrays require driving and interface circuitry, and in most cases this circuitry is analog rather than digital, making the circuitry capable of delivering or sensing a range of input signals. However, in many applications the video signal originates in digital form and must be converted to analog form to drive the display. Suitable digital-to-analog (DAC) conversion circuitry can be built using well-known techniques in conventional silicon integrated circuits (ICs). These ICs are mounted on or adjacent to the substrate containing the pixel array and a large number of electrical connections are made between the two. The cost of the peripheral drive, interface chips, mounting, and electrical connections to the display can constitute a significant proportion of the overall cost of a system containing the display.

SUMMARY

If the ICs and connections can be eliminated or greatly reduced by integrating suitable circuitry on the substrate, then the system cost can be reduced and its reliability improved.

An apparatus and method can convert digital data to analog data using column load capacitances on adjacent pairs of column lines of the LCD. The apparatus can include a data bus containing digital data. A row buffer can be coupled to the data bus for receiving and distributing the digital data. A switch network can be coupled to the row buffer for converting the digital data received from the row buffer to analog data using column load capacitances on adjacent pairs of column lines of the LCD.

The switch network can include a plurality of switching devices, where each switching device can be coupled to an adjacent respective pair of column lines of the

LCD. Each switching device can include a logic circuit which can receive digital data from the row buffer and at least three MOSFETs which can convert the received digital data received from the logic circuit to analog data and transmit the analog data through respective column lines. The MOSFETs can be n-channel MOSFETs, p-channel MOSFETs, or a combination of n-channel and p-channel MOSFETs.

A first column line of the pair of column lines can be coupled to alternating pixels in a first column of pixels and a second column line of the pair of column lines can be coupled to alternating pixels in a second column of pixels. The pixels of the first column line can be in alternating rows with respect to the pixels in the second column line.

The pixels can be arranged in a rectangular layout for a black and white display or the pixels can be arranged in a delta layout for a color display.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of particular embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is a schematic representation of a prior art data scanner;

Fig. 2A is a schematic representation of a typical pixel layout for a black and white (B/W) display for the data scanner of Fig. 1;

Fig. 2B is a schematic representation of a typical pixel layout for a color display for the data scanner of Fig. 1;

Fig. 2C is a circuit diagram of a typical pixel of Figs. 2A and 2B;

Figs. 3A-3I are circuit diagrams of a DAC of Fig. 1 converting a digital signal to an analog signal;

Fig. 4 is a schematic representation of a data scanner according to an embodiment of the present invention;

Fig. 5A is a schematic representation of a typical pixel layout for a B/W display for the data scanner of Fig. 4;

Fig. 5B is a schematic representation of a typical pixel layout for a color display for the data scanner of Fig. 4; and

Fig. 6 is a circuit diagram of a switch device of Fig. 4.

DETAILED DESCRIPTION

Fig. 1 shows a data scanner 50 and column load capacitances 160 of an LCD 100. The data scanner 50 includes integrated DACs 140 and amplifiers 150 to drive the column load capacitance 160 of the display 100. The configuration can be used to drive the column load capacitances 160 of black and white (B/W) or color displays. Generally, a row buffer 110 distributes digital data arriving from a data bus 130 to the DACs 140 on a pulse received from a clock 120. The DACs 140 operate in parallel and receive the digital data and convert the digital data to analog signals. Because the DACs 140 typically provide a high impedance output, display applications need the amplifiers 150 to drive the column load capacitance 160. In particular, the switched-capacitor DACs 140 require the amplifiers 150 because the column load capacitances 160 are typically greater than practically realizable DAC capacitors 330, 340 (Figs. 3A-3I). Thus, the amplifiers 150 provide a greater output to the column load capacitances 160 of column lines 135 of the display 100.

Fig. 2A shows a typical pixel array and column line 135 layout for a display 100 with pixels 200 in a "rectangular" arrangement, while Fig. 2B shows a typical pixel array and column line 135 layout for a display 100 with pixels in a "delta" arrangement. The "rectangular" arrangement is commonly used for B/W displays, while the "delta" arrangement is commonly used for color displays. The letters RGB stand for Red, Green, and Blue and are well known in the art for color displays. Rectangular pixels 200 are used in both black-and-white and color displays, typically with square pixels for monochrome and rectangular stripes (height:width ratio = 3:1) for color.

Fig. 2C shows a circuit diagram of a typical pixel 200 as shown in Figs. 2A and 2B. The typical pixel 200 includes a MOSFET transistor 220 and a capacitor 160.

Each pixel 200 is connected to a row line 210 and a column line 135. The row line 210 controls the gate of MOSFET 220, which turns the pixel on and off. When the MOSFET 220 is turned on, the pixel 200 is driven by the column load capacitance 160 (FIG. 1) on the column line 135.

Figs. 3A-3I shows a switched-capacitor DAC 140 converting a digital signal to an analog signal. The simple bit-serial DAC 140 includes two capacitors 330, 340 and two switches 310, 320. Switch 310 may be connected high, connected low, or left open. Switch 320 may connect the top plates of capacitors 330 and 340 or may be left open. Bit-parallel DACs using more capacitors and appropriate switch configurations can also be used. In this example, as illustrated sequentially in Figs. 3A-3I, a 16 bit digital input code, 1101 or 16 decimal, is converted to an analog signal which is 13/16 V_{FS}, where V_{FS} = full-scale output voltage.

Numerous problems arise when using switch-capacitor DACs 140 and associated amplifiers 150 (Fig. 1). First, the capacitors 330, 340 of the DACs 140 must be well-matched for predictable charge sharing. The example of Figs. 3A-3I relies on the capacitors 330, 340 being equal, so that the charge is shared equally when switch 320 is closed. Second, it is hard to integrate DACs 140 on fine pitch column lines 135 because more area is needed for well-matched DAC capacitors 330, 340. If the DAC capacitors 330, 340 are too small, then undesirable parasitic capacitances become more significant. Third, it is hard to integrate numerous amplifies 150 (Fig. 1) on the display 100 because the amplifiers 150 need to be low power, have good matching (i.e., to prevent vertical lines in the image), and be integrated with fine pitch column lines. Lastly, multiplexers may need to be used to share DACs 140 and amplifiers 150 because of size restrictions, adding more complexity to the display 100.

Embodiments of the present invention eliminate the need for specific switched-capacitor DACs 140 and their associated amplifiers 150. As shown in Fig. 4, the DACs 140 and amplifiers 150 (Figs. 1-3I) of the data scanner 50 are replaced by a switch network that utilizes the column line capacitances 160 to convert the digital signals to analog signals. That is, new switched capacitor DACs are constructed using the switch network and the column load capacitances 160 as the DAC capacitors. In this

configuration, a row buffer 110 distributes digital data arriving from a data bus 130 to switches 410 on a pulse received from a clock 120. The switches 410 convert the digital data to analog signals using the column load capacitances 160 of an adjacent pair of column lines 135.

Fig. 5A shows pixel array layout connections required to convert the digital signal to an analog signal using the switch 410 and column load capacitances 160 for B/W displays, while Fig. 5B shows pixel array layout connections for color displays. As shown, a rectangular layout is commonly used for B/W displays and a "delta" layout is commonly used for color displays. Each column line pair 500 is connected to one pixel 200 per row. The column pairs 500 have matched column capacitances if they have the same number of left and right connected pixels 200. The use of column line pairs 500 suggests more display area, which reduces the active pixel aperture. However, in anticipated technology, the pixel aperture is limited by optical, LC, and other issues and not by the interconnect pitch.

Fig. 6 shows a circuit diagram of the switch 410 of Fig. 4. The switch 410 includes five MOSFET transistors 610, 620, 630, 640, and 650. The gates of each MOSFET are connected to a logic circuit 660. The logic circuit 660 contains the digital data received from the row buffer 110 (FIG. 4) and distributes the digital data to the MOSFETs. MOSFETs 610 and 630 perform a similar operation of switch 310 of FIG. 3. MOSFET 610 can drive the column high to VFS, MOSFET 630 can drive it low, or both MOSFETs can be turned off for an open connection. Similarly, MOSFET 650 performs a similar operation of switch 320 of FIG. 3, connecting the two columns to equalize charge. Optional MOSFETs 620 and 640 are provided for symmetry to MOSFETs 610 and 630. The circuit can be operated with MOSFETs 610 and 630 driving the left column line while, charge is accumulating on the right column line, or else with MOSFETs 620 and 640 driving the right column line, while charge is accumulating on the left column line.

FIG. 6 uses n-channel MOSFETs for switches. However, P-channel MOSFET or complementary pairs of n- and p-channel MOSFETs may also be used. Additional MOSFETs may be used for charge injection cancellation, using the well-known

technique in which both source and drain of a compensating MOSFET are connected to the high-impedance side of the switch, and in which the gate of the compensating MOSFET is driven with the logical inverse of the gate of the switch MOSFET, and in which the compensating MOSFET is one half the size of the switch MOSFET.

While this invention has been particularly shown and described with references to particular embodiments, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the scope of the invention encompassed by the appended claims.